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EXAMINER

TOLEDO, FERNANDO L

ART UNIT PAPER NUMBER

2823

DATE MAILED: 02/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/816,393

Applicant(s)

MATSUOKA, FUNITOMO

Examiner

Fernando Toledo

Art Unit

2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 November 2002.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3,5-10 and 12-18 is/are pending in the application.
- 4a) Of the above claim(s) 14-18 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3,5-10,12 and 13 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 March 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☒ The proposed drawing correction filed on 29 November 2002 is: a) ☒ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 8.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

Art Unit: 2823

DETAILED ACTION

Drawings

1. The corrected or substitute drawings were received on 29 November 2002. These drawings are acceptable.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1 – 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (hereinafter AAPA) in view of Yu (U. S. patent 6,225,173 B1).

In re claim 1, AAPA discloses forming a dummy gate electrode on a semiconductor substrate having a predetermined length coincident with a length of a gate electrode to be formed (figure 1); with the dummy gate electrode used as a mask, forming one pair of first impurity diffusion layers in regions of the semiconductor substrate which are opposite to each other on opposite sides of the dummy gate electrode (figure 1); forming an insulating film on the semiconductor substrate in a way to bury the dummy gate electrode, while exposing an upper surface of the gate electrode (figure 4); removing the dummy gate electrode and forming a first trench in the insulating film having a width corresponding to at least the predetermined length of the dummy gate electrode

Art Unit: 2823

(figure 4); lining the gate insulating film of the thickness along the inner surface of the second trench (figure 7); forming the gate electrode in the second trench with only the gate insulating film intervening therebetween (figure 8).

AAPA does not show, enlarging the width of the first trench and forming a second trench in the insulating film, which is greater in width than the width of the first trench.

However, Yu, in the U. S. patent 6,225,173 B1; figures 1 – 5 and related text, disclose enlarging the width of the first trench and forming a second trench in the insulating film, which is greater in width than the width of the first trench (figures 4 and 5) to form an ultra-shallow source extension and an ultra-shallow drain extension (column 2).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to enlarge the width of the first trench and forming a second trench in the insulating film, which is greater in width than the width of the first trench, in the AAPA invention, because, as taught by Yu, it forms an ultra-shallow source extension and an ultra-shallow drain extension.

In re claim 2, AAPA discloses after forming the first impurity diffusion layers, forming a side wall insulating film on a side wall surface of the dummy gate electrode (figure 2); and with the dummy gate electrode and the side wall insulating film used as a mask, forming second impurity diffusion region layers having a deeper junction in the semiconductor substrate than the first impurity diffusion layers (figure 2).

Art Unit: 2823

In re claim 3, Yu discloses wherein the step of forming a second trench includes a step of performing an isotropic etching on the insulating film having the first trench formed therein (column 4).

In re claim 4, AAPA discloses the step of forming a gate insulating film includes a step of forming a gate insulating film in a manner to make the width of the second trench equal to, or greater than, that of the first trench (page 5).

In re claim 5, AAPA discloses wherein the step of forming the gate insulating layer includes a step of using an insulating material having a relative dielectric constant of above 5 (page 5).

In re claim 6, AAPA discloses wherein the step of forming a gate insulating film includes a step of using one selected from the group consisting of Ta_2O_5 , silicon nitride, Al_2O_3 , BaSrTiO_3 , Zr oxide, Hf oxide, Sc oxide, Y oxide and Ti oxide.

In re claim 7, AAPA discloses forming a first insulating film on a semiconductor substrate (figure 1); sequentially forming a first semiconductor film and a second insulating film on the first insulating film (figure 1); forming a resist pattern on the second insulating film (figure 1); with the resist pattern used as a mask, patterning the first semiconductor film and the second insulating film by an anisotropic etching to provide a stacked layer structure of the first semiconductor film and the second insulating film on the semiconductor substrate having a predetermined width coincident with a length of a gate electrode to be formed (figure 1); with the stacked layer structure used as a mask, ion-implanting an impurity in the semiconductor substrate to provide first impurity diffusion layers

Art Unit: 2823

for a source and a drain (figure 1); forming a third insulating film over the semiconductor structure to bury the stacked layer structure (figure 4); etching back the third film to expose an upper surface of the stacked layer structure (figure 4); with the third insulating film used as a mask, removing the stacked layer structure to form a trench in the third insulating film (figure 4); depositing a fourth insulating film along an inner surface of the trench (figure 7); forming a conductive layer on and in contact with the fourth insulating film to form the gate electrode of a length coincident with the predetermined width (figure 8).

AAPA does not show, enlarging the width of the first trench and forming a second trench in the insulating film, which is greater in width than the width of the first trench.

However, Yu, in the U. S. patent 6,225,173 B1; figures 1 – 5 and related text, disclose enlarging the width of the first trench and forming a second trench in the insulating film, which is greater in width than the width of the first trench (figures 4 and 5) to form an ultra-shallow source extension and an ultra-shallow drain extension (column 2).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to enlarge the width of the first trench and forming a second trench in the insulating film, which is greater in width than the width of the first trench, in the AAPA invention, because, as taught by Yu, it forms an ultra-shallow source extension and an ultra-shallow drain extension.

In re claim 8, AAPA discloses after providing the first impurity diffusion layers, forming a sidewall insulating film on a sidewall of the stacked layer

Art Unit: 2823

structure (figure 2); with the sidewall insulating film and the stacked layer structure used as a mask, forming second impurity diffusion layers having a deeper junction in the semiconductor substrate than the first diffusion layers (figure 2).

In re claim 9, AAPA in view of Yu does not teach wherein the step of enlarging the width of the trench includes a step of using, as the isotropic etching, an etching treatment including HF and NH_4F .

However, It would have been obvious to one having ordinary skill in the art at the time the invention was made to use in the isotropic etching to enlarge the width of the trench an etching treatment including HF and NH_4F since it has been held to be within the general skill of a worker in the art to select a known material on the base of its suitability, for its intended use involves only ordinary skill in the art.

In re Leshin, 125 USPQ 416.

In re claim 10, AAPA discloses depositing a fourth insulating film by a CVD or a sputtering method (page 5).

In re claim 11, AAPA discloses wherein the step of depositing a fourth insulating film includes a step of forming the fourth insulating film to make the width of the trench after forming the fourth insulating film equal to, or greater than, that of the first trench (page 6).

In re claim 12, AAPA discloses wherein the step of forming the gate insulating layer includes a step of using an insulating material having a relative dielectric constant of above 5 (page 5).

Art Unit: 2823

In re claim 13, AAPA discloses wherein the step of forming a gate insulating film includes a step of using one selected from the group consisting of Ta₂O₅, silicon nitride, Al₂O₃, BaSrTiO₃, Zr oxide, Hf oxide, Sc oxide, Y oxide and Ti oxide.

Response to Arguments

3. Applicant's arguments filed 29 November 2002 have been fully considered but they are not persuasive for the foregoing reasons.

4. Applicant contests that the rejection under 35 USC §103 is improper because there is no admission of prior art either in the drawings or in the specification as filed. "Furthermore, the case law requires that an actual admission of 'prior art' status must be made to establish such status."

The Examiner respectfully submits the following evidence taken from the specification as filed that establishes such status: Page 1 of the specification as filed, line 17 – 20 discloses the following: "A *conventional* manufacturing process for manufacturing a MISFET using a buried type gate electrode will be explained below with reference to FIGS. 1 to 8." Page 6 of the specification as filed, line 5 discloses the following: "In the *prior art* technique, as set out above." The Examiner believes these remarks as sufficient evidence to state that FIGS. 1 – 8 are in fact recognized as prior art. Therefore, Applicant's arguments contesting such validity are moot.

5. Applicant contests that Yu does not teach that the gate length of the dummy gate electrode correspond to the final gate electrode length.

Art Unit: 2823

Examiner respectfully submits that the teachings of Yu are to show the enlargement of the trench so as to form the ultra shallow source and drain extensions, and that AAPA does show that the gate length of the dummy gate electrode corresponds to the final gate electrode length. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Therefore the rejection is not overcome by pointing out that one reference does not contain a particular teaching when the relevance for that teaching was on the other reference. In *Re Lyons* 150 PQ41. Unobviousness cannot be established by attacking references individually when rejection is based on combination of references. *Ex Parte Campkell* 172 USPQ 91, *In Re Young* 159 USPQ 725.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory

Art Unit: 2823

action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fernando Toledo whose telephone number is 703-305-0567. The examiner can normally be reached on Mon-Fri 8am to 4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7382 for regular communications and 703-308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Fernando Toledo
Examiner
Art Unit 2823

ft
January 31, 2003


Olik Chaudhuri
Supervisory Patent Examiner
Technology Center 2800